A TWO-STAGE MONOLITHIC BUFFER AMPLIFIER FOR 20 GHz SATELLITE COMMUNICATION

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ABSTRACT

Design, fabrication, and test results of a two-stage GaAs monolithic buffer amplifier for 20 GHz satellite communication are described in this paper. A gain of 13 ± 0.75 dB from 17.7 to 20.2 GHz was obtained from the 1.5 × 1.5 millimeter chip, which includes all necessary bias and dc blocking circuitry.

INTRODUCTION

Rockwell International is currently developing a 20 GHz Monolithic Transmit Module for NASA,* which consists of a five bit phase shifter (with control logic) and a power amplifier. A key component of this transmit module is the low power buffer amplifier needed to overcome losses in the passive phase shifter. A conservative design approach was selected which requires the use of two amplifying stages, providing a total gain of at least 12 dB across the 17.7 to 20.2 GHz band. This paper describes current status of the buffer amplifier, which will soon become a component on a larger monolithic chip. Circuit design considerations, fabrication techniques, and measured results will be described in the following sections of this paper.

CIRCUIT DESIGN

Design goals for the buffer amplifier are a gain of at least 12 dB with an input and output VSWR of 1.5:1 or better. In addition, the bias circuit and processing sequence must be compatible with other analog and digital components on the monolithic transmit module. Chip area must be minimized to obtain reasonable chip size for the overall monolithic module under development. On chip input and output blocking capacitors are needed to avoid interference with the phase shifter and input drive circuitry.

The design process begins with development of an FET small signal model. Center fed 200 micron wide FETs were selected for this application; however all modeling begins from the model of a single 100 micron wide by 0.75 micron long gate finger. A complete FET model is then constructed from the gate finger model and passive parasitic interconnecting elements. This compound FET model is then used for initial circuit design. After a preliminary layout is generated, parasitic elements caused by layout geometry are included in the circuit analysis file and relevant circuit parameters are re-optimized. After several iterations a layout is obtained which is consistent with acceptable predicted performance.

Table 1 shows calculated S-parameters of the 100 micron wide FET finger used for design of the 20 GHz buffer. Note that the device is potentially unstable up to almost 30 GHz, which is characteristic of all high performance FETs, and that ample gain is available for the task at hand. Figure 1 is a schematic of the amplifier and Fig. 2 shows a photograph of the actual chip. Figure 3 is a plot of predicted gain vs frequency. Included in this calculation are parasitic interelement capacitive coupling and chip via hole inductances. Although not visible from the chip photograph, there are six thru substrate via holes in the 1.5 × 1.5 millimeter chip, which is 0.125 millimeters thick. Each via hole has an estimated 0.07 nH of inductance associated with it, which can have a significant effect on amplifier performance at 20 GHz. Careful layout is necessary to simultaneously provide sufficient mechanical strength and adequate RF grounding of the circuit.

Table 1

S-Parameters

F (GHz)	S11	S21	S12	S22
15.0	0.92 < -42.1	0.83 < 128.8	0.092 < 63.0	0.86 < -16.1
16.0	0.91 < -44.6	0.83 < 125.8	0.097 < 61.0	0.85 < -17.1
17.0	0.90 < -47.0	0.82 < 122.8	0.102 < 60.0	0.85 < -18.0
18.0	0.89 < -49.4	0.81 < 119.8	0.106 < 58.0	0.85 < -18.9
19.0	0.88 < -51.7	0.80 < 116.9	0.110 < 57.0	0.84 < -19.9
20.0	0.88 < -54.0	0.79 < 114.1	0.114 < 56.0	0.84 < -20.7
21.0	0.87 < -56.2	0.78 < 111.4	0.118 < 54.0	0.83 < -21.6
22.0	0.86 < -58.3	0.78 < 108.6	0.121 < 53.0	0.83 < -22.5
23.0	0.85 < -60.4	0.77 < 106.0	0.125 < 52.0	0.83 < -23.3
24.0	0.84 < -62.5	0.76 < 103.4	0.128 < 51.0	0.82 < -24.1
25.0	0.83 < -64.5	0.75 < 100.9	0.131 < 49.0	0.82 < -25.0

The design of this two-stage amplifier has several noteworthy features. The FETs share a common dc drain supply but have independent gate bias lines. This allows independent current

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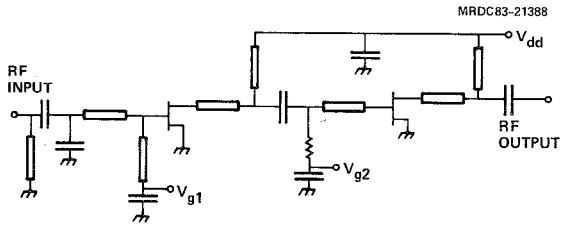

Fig. 1 Schematic of the 20 GHz monolithic amplifier.

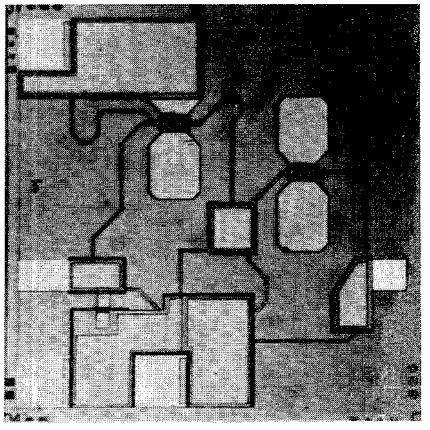

Fig. 2 Photograph of two-stage 20 GHz buffer amplifier.

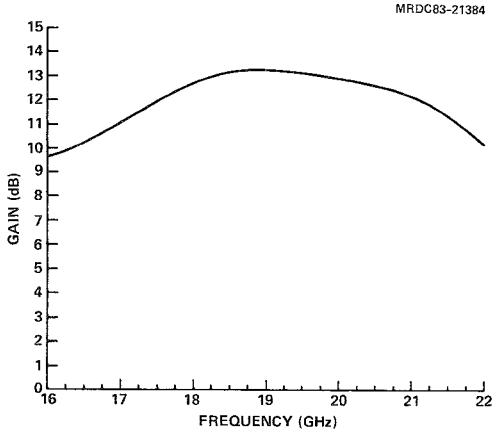

Fig. 3 Predicted gain of the two-stage monolithic amplifier.

adjustment, however, since an interstage blocking capacitor is provided they can also be operated from a common supply. Shorted stubs at each gate and one near the output serve the dual purposes of RF tuning and bias insertion. The gate of the second FET is biased via a 10K resistor since additional inductive tuning is not needed at that location. RF chokes or quarter wave lines would consume too much valuable real estate.

Sensitivity to variations in element values is also of interest. The three parameters most subject to process variations are the FET input capacitance, the FET transconductance, and the chip thickness. Shown in Fig. 4 are the gain curves for a ± 10% variation of each parameter. Figure 4a shows that gain varies approximately proportionally to transconductance which is expected from any tuned amplifier without intentional feedback. Variations in FET input capacitance cause larger variations at the high end of the band than at the low end, indicating that this parameter must be more precisely controlled. This is shown in Fig. 4b. Substrate thickness variations are not as significant, as shown in Fig. 4c; however large variations from wafer to wafer must be avoided.

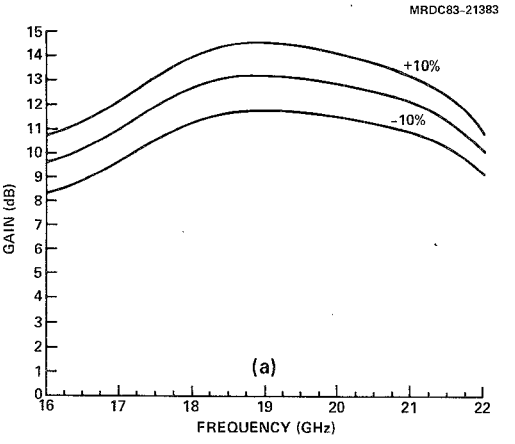

Fig. 4a Gain sensitivity to FET transconductance.

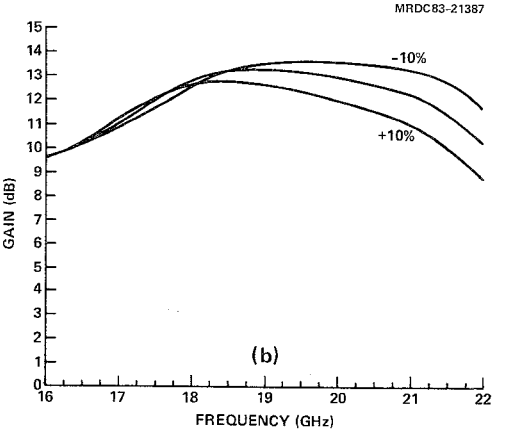

Fig. 4b Gain sensitivity to FET input capacitance.

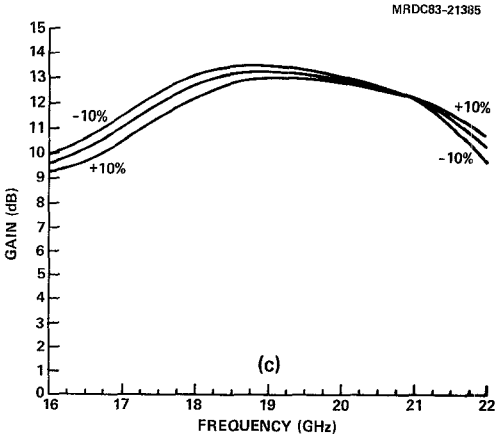

Fig. 4c Gain sensitivity to substrate thickness variations.

CIRCUIT FABRICATION

Fabrication of the 20 GHz amplifier begins with the synthesis of doping profiles for FET active layers, n^+ contacts, and the bulk resistor used for biasing. Localized Si^+ ion implantation in qualified semi-insulating substrates is used for this step. AuGe/Ni ohmic contacts are then defined by photolithography and alloyed to contact the FET active layer and the bias resistor. A recessed T-bar gate structure is then formed by either contact photolithography or electron beam lithography. The measured results presented in this paper were obtained from chips fabricated by contact lithography. First layer metallization used for some interconnects and the bottom plate of the metal-insulator-metal (MIM) capacitors is then defined, followed by fabrication of the low capacitance polyimide bridges and deposition of the Si_3N_4 insulator portion of the MIM capacitors. A second metallization layer formed by electroplating then completes the front side processing. Wafer thinning, etching of the via holes, back side plating, and sawing then yields amplifiers ready for test. Details of the fabrication procedure are outlined in Reference 2.

MEASURED PERFORMANCE

Measured gain of the 20 GHz buffer amplifier is shown in Fig. 5 (curve B) superimposed on the predicted gain (curve A) from Fig. 3. Curve B in Fig. 5 was obtained from a swept power meter referenced to a short length of 50 ohm microstrip mounted in the test fixture described in Reference 1. All measurements described in this paper were performed using this test fixture. Resonances in the measured data are believed to be caused by VSWR interactions in the test setup and are not due to on chip resonances. Curve C, measured in the same fixture on a full vector correcting 18 GHz Automatic Network Analyzer (ANA) tends to support this hypothesis. Accurate full band gain measurement as well as input and output VSWR measurements must await completion of Rockwell's 20 GHz ANA.

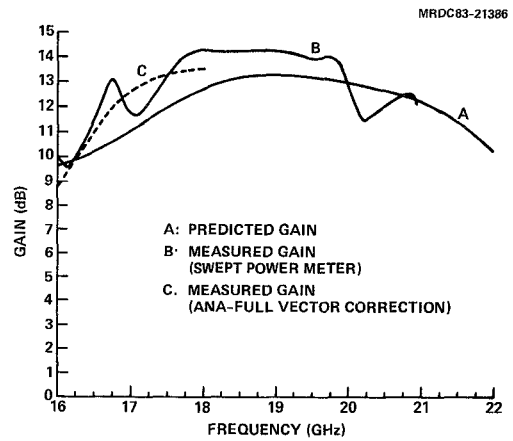

Fig. 5 Measured gain of the 20 GHz two-stage amplifier.

It should also be noted that this amplifier is potentially unstable, which can complicate measurement in a waveguide test set. Careful control of bias circuitry and below band source and load impedance is needed to avoid oscillation. Although not included in the initial design, future implementations will include on chip stabilization circuitry to eliminate potential oscillation problems in the transmit module chip.

CONCLUSION

A monolithic two-stage 20 GHz buffer amplifier has been designed and fabricated as a key component of a 20 GHz monolithic transmit module. Over 12 dB of gain was obtained from 17.7 to 20.2 GHz on a compact 1.5 × 1.5 millimeter GaAs chip. Measurement difficulties have highlighted the necessity of accurate and versatile test fixtures and the requirements for computer correction of the measured data.

REFERENCES

1. J.A. Benet, "The Design and Calibration of a Universal MMIC Test Fixture," IEEE 1982 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest of Papers, pp. 36-41, June 1982.
2. A.K. Gupta, W.C. Petersen and D.R. Decker, "Yield Considerations for Ion Implanted GaAs MMICs," to be published in the January 1983 issue of the IEEE Transactions on MTT.